# BCP69T1G

# PNP Silicon Epitaxial Transistor

This PNP Silicon Epitaxial Transistor is designed for use in low voltage, high current applications. The device is housed in the SOT−223 package, which is designed for medium power surface mount applications.

**Features**

- High Current: $I_C$ = −1.0 A
- The SOT−223 Package Can Be Soldered Using Wave or Reflow.
- SOT−223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die.
- NPN Complement is BCP68
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | −20 | Vdc |
| Collector−Base Voltage | $V_{CBO}$ | −25 | Vdc |
| Emitter−Base Voltage | $V_{EBO}$ | −5.0 | Vdc |
| Collector Current | $I_C$ | −1.0 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1)<br>Derate above 25°C | $P_D$ | 1.5<br>12 | W<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −65 to 150 | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance − Junction−to−Ambient (Surface Mounted) | $R_{\theta JA}$ | 83.3 | °C/W |
| Lead Temperature for Soldering, 0.0625 in from case<br>Time in Solder Bath | $T_L$ | 260<br>10 | °C<br>s |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 sq. in.

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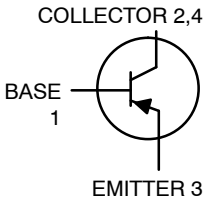
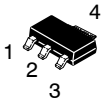
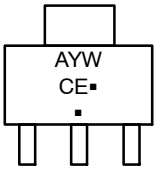
**MEDIUM POWER PNP SILICON HIGH CURRENT TRANSISTOR SURFACE MOUNT**




**SOT−223 (TO−261)**
**CASE 318E**
**STYLE 1**

**MARKING DIAGRAM**




CE = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| BCP69T1G | SOT−223 (Pb−Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Emitter Breakdown Voltage ($I_C$ = −100 μAdc, $I_E$ = 0) | $V_{(BR)CES}$ | −25 | − | − | Vdc |
| Collector−Emitter Breakdown Voltage ($I_C$ = −1.0 mAdc, $I_B$ = 0) | $V_{(BR)CEO}$ | −20 | − | − | Vdc |
| Emitter−Base Breakdown Voltage ($I_E$ = −10 μAdc, $I_C$ = 0) | $V_{(BR)EBO}$ | −5.0 | − | − | Vdc |
| Collector−Base Cutoff Current ($V_{CB}$ = −25 Vdc, $I_E$ = 0) | $I_{CBO}$ | − | − | −10 | μAdc |
| Emitter−Base Cutoff Current ($V_{EB}$ = −5.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | − | − | −10 | μAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain<br>($I_C$ = −5.0 mAdc, $V_{CE}$ = −10 Vdc)<br>($I_C$ = −500 mAdc, $V_{CE}$ = −1.0 Vdc)<br>($I_C$ = −1.0 Adc, $V_{CE}$ = −1.0 Vdc) | $h_{FE}$ | <br>50<br>85<br>60 | <br>−<br>−<br>− | <br>−<br>375<br>− | − |
| Collector−Emitter Saturation Voltage ($I_C$ = −1.0 Adc, $I_B$ = −100 mAdc) | $V_{CE(sat)}$ | − | − | −0.5 | Vdc |
| Base−Emitter On Voltage ($I_C$ = −1.0 Adc, $V_{CE}$ = −1.0 Vdc) | $V_{BE(on)}$ | − | − | −1.0 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Current−Gain − Bandwidth Product<br>($I_C$ = −10 mAdc, $V_{CE}$ = −5.0 Vdc) | $f_T$ | − | 60 | − | MHz |

## TYPICAL ELECTRICAL CHARACTERISTICS

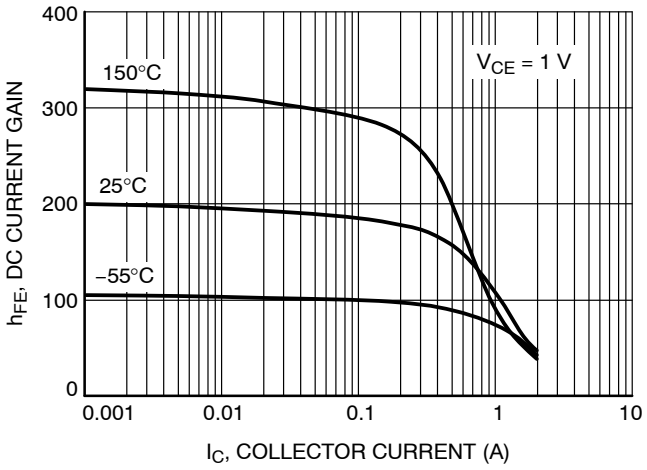



**Figure 1. DC Current Gain**

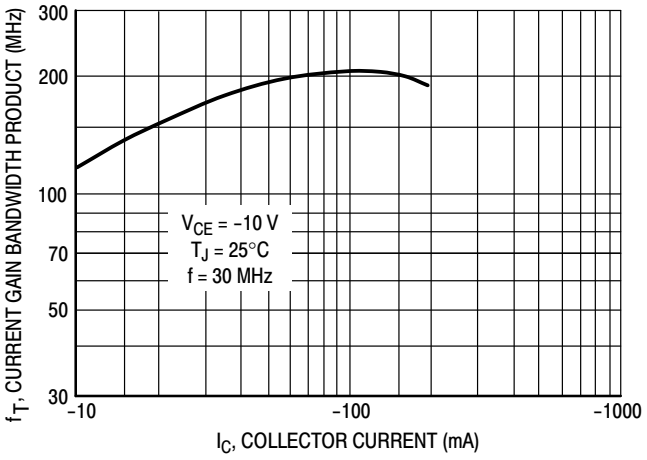



**Figure 2. Current Gain Bandwidth Product**

## TYPICAL ELECTRICAL CHARACTERISTICS

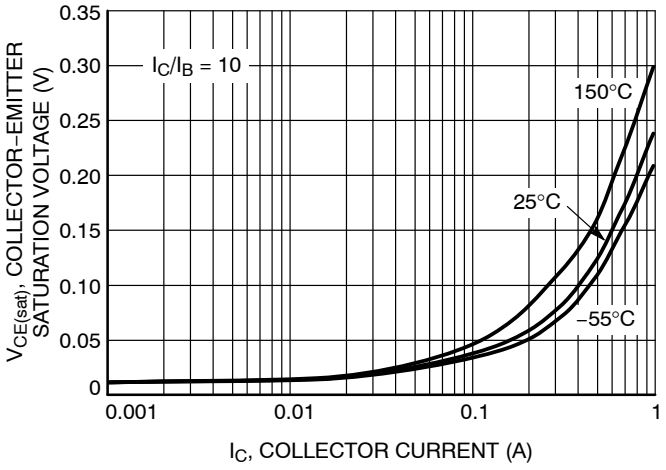



**Figure 3. Collector Emitter Saturation Voltage vs. Collector Current**

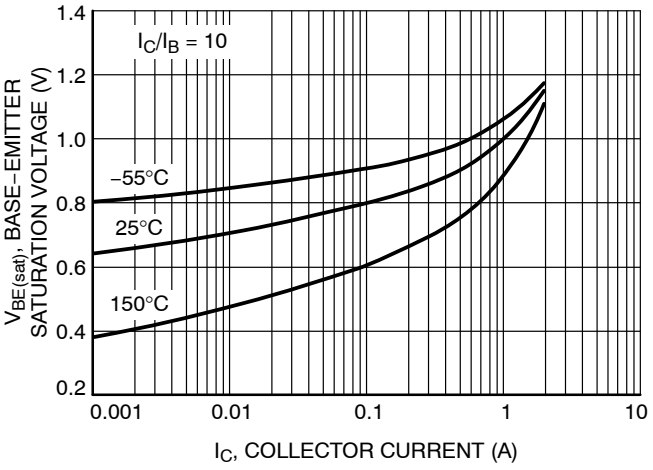



**Figure 4. Base Emitter Saturation Voltage vs. Collector Current**

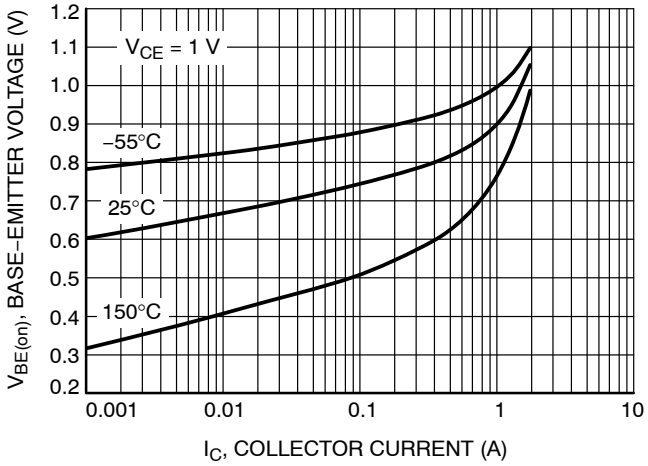



**Figure 5. Base Emitter Voltage vs. Collector Current**

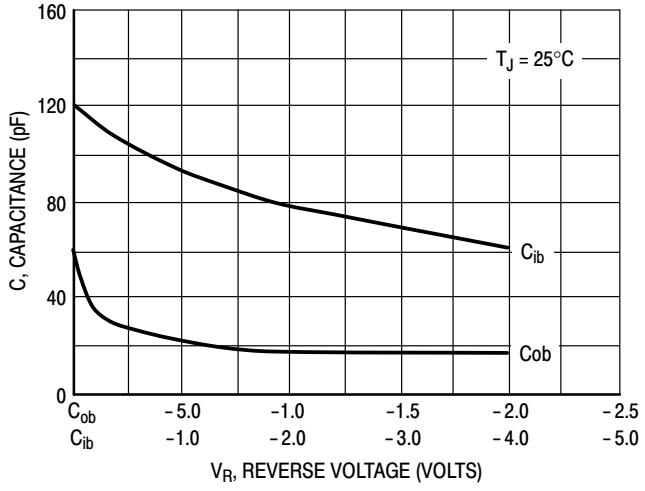



**Figure 6. Capacitances**

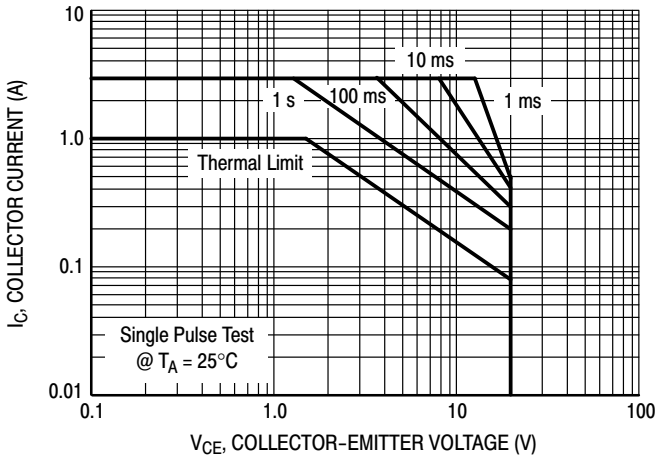
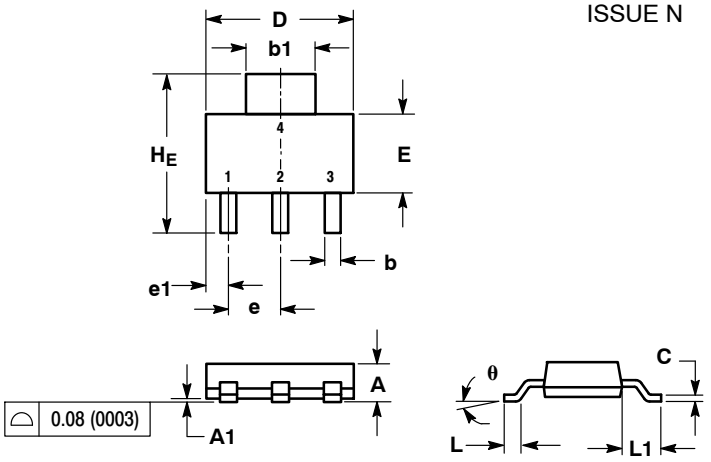



**Figure 7. Safe Operating Area**

## PACKAGE DIMENSIONS

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE N

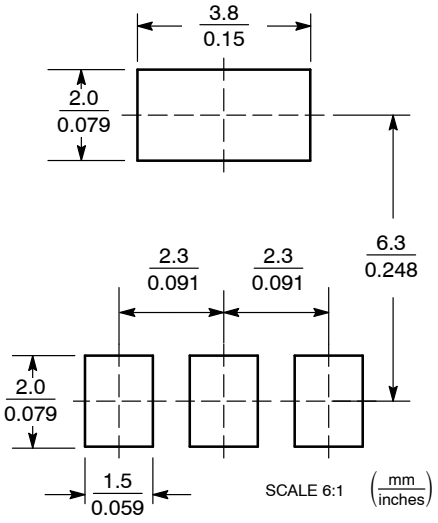



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.50 | 1.63 | 1.75 | 0.060 | 0.064 | 0.068 |
| A1 | 0.02 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.60 | 0.75 | 0.89 | 0.024 | 0.030 | 0.035 |
| b1 | 2.90 | 3.06 | 3.20 | 0.115 | 0.121 | 0.126 |
| c | 0.24 | 0.29 | 0.35 | 0.009 | 0.012 | 0.014 |
| D | 6.30 | 6.50 | 6.70 | 0.249 | 0.256 | 0.263 |
| E | 3.30 | 3.50 | 3.70 | 0.130 | 0.138 | 0.145 |
| e | 2.20 | 2.30 | 2.40 | 0.087 | 0.091 | 0.094 |
| e1 | 0.85 | 0.94 | 1.05 | 0.033 | 0.037 | 0.041 |
| L | 0.20 | −−− | −−− | 0.008 | −−− | −−− |
| L1 | 1.50 | 1.75 | 2.00 | 0.060 | 0.069 | 0.078 |
| $H_E$ | 6.70 | 7.00 | 7.30 | 0.264 | 0.276 | 0.287 |
| θ | 0° | – | 10° | 0° | – | 10° |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



### PUBLICATION ORDERING INFORMATION

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